

WHAT IS CLAIMED IS:

1 1. A demodulator for demodulating a set of S possible
2 orthogonal modulation codes received serially as binary data,
3 wherein each of said orthogonal modulation codes comprises M binary
4 bits representing an N-bit data symbol and wherein $M = 2^N$, said
5 demodulator comprising:

6 a Logic 0 input detector capable of comparing each of
7 said M binary bits of said serially received orthogonal modulation
8 codes to a Logic 0 and outputting a +1 signal if a match occurs and
9 outputting a -1 signal if a match does not occur;

10 a summation circuit comprising S accumulators;

11 a Logic 0 switch array comprising S switches, wherein a
12 Kth one of said S switches in said Logic 0 switch array is capable
13 of coupling an output of said Logic 0 input detector to a first
14 input of a Kth one of said S accumulators;

15 a storage array capable of storing said S orthogonal
16 modulation codes; and

17 control circuitry capable of synchronously applying the
18 M bits in a Kth one of said S orthogonal modulation codes in said
19 storage array as a switch control signal to said Kth switch in said
20 Logic 0 switch array so that each Logic 0 binary data in said Kth
21 orthogonal modulation code closes said Kth switch in said Logic 0

switch array, thereby connecting the output signal of said Logic 0 input detector to said first input of said Kth accumulator.

2. The demodulator as set forth in Claim 1 further comprising:

a Logic 1 input detector capable of comparing each of said M binary bits of said serially received orthogonal modulation codes to a Logic 1 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur; and

a Logic 1 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 1 switch array couples an output of said Logic 1 input detector to a second input of said Kth accumulator;

wherein said control circuitry is capable of synchronously applying the M bits in said Kth orthogonal modulation code in said storage array as a switch control signal to said Kth switch in said Logic 1 switch array so that each Logic 1 binary data in said Kth orthogonal modulation code closes said Kth switch in said Logic 1 switch array, thereby connecting the output signal of said Logic 1 input detector to said second input of said Kth accumulator.

1 3. The demodulator as set forth in Claim 2 wherein each
2 Logic 1 binary data in said Kth orthogonal modulation code opens
3 said Kth switch in said Logic 0 switch array, thereby disconnecting
4 the output signal of said Logic 0 input detector from said first
5 input of said Kth accumulator.

1 4. The demodulator as set forth in Claim 3 wherein each
2 Logic 0 binary data in said Kth orthogonal modulation code opens
3 said Kth switch in said Logic 1 switch array, thereby disconnecting
4 the output signal of said Logic 1 input detector from said second
5 input of said Kth accumulator.

1 5. The demodulator as set forth in Claim 2 further
2 comprising a code selection circuit capable of reading a sum value
3 from each said S accumulators and identifying an accumulator
4 containing a maximum sum value.

1 6. The demodulator as set forth in Claim 5 wherein said code
2 selection circuit outputs one of 2^N N-bit data symbols
3 corresponding to said identified accumulator contain said maximum
4 value.

1 7. The demodulator as set forth in Claim 6 wherein $N = 6$ and
2 $M = 2^N = 64$.

1 8. The demodulator as set forth in Claim 7 wherein $S = 64$.

1 9. The demodulator as set forth in Claim 8 wherein said
2 orthogonal modulation codes are Walsh codes.

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1 10. A code division multiple access (CDMA) wireless network
2 comprising a plurality of base transceiver stations capable of
3 communicating with access terminals located in a coverage area of
4 said wireless network, wherein a first one of said plurality of
5 base transceiver stations comprises:

6 a demodulator for demodulating a set of S possible
7 orthogonal modulation codes received serially as binary data,
8 wherein each of said orthogonal modulation codes comprises M binary
9 bits representing an N-bit data symbol and wherein $M = 2^N$, said
10 demodulator comprising:

11 a Logic 0 input detector capable of comparing each
12 of said M binary bits of said serially received orthogonal
13 modulation codes to a Logic 0 and outputting a +1 signal if a
14 match occurs and outputting a -1 signal if a match does not
15 occur;

16 a summation circuit comprising S accumulators;

17 a Logic 0 switch array comprising S switches,
18 wherein a Kth one of said S switches in said Logic 0 switch
19 array is capable of coupling an output of said Logic 0 input
20 detector to a first input of a Kth one of said S accumulators;

21 a storage array capable of storing said S orthogonal
22 modulation codes; and

1 11. The CDMA wireless network as set forth in Claim 10
2 further comprising:

3 a Logic 1 input detector capable of comparing each of
4 said M binary bits of said serially received orthogonal modulation
5 codes to a Logic 1 and outputting a +1 signal if a match occurs and
6 outputting a -1 signal if a match does not occur; and

7 a Logic 1 switch array comprising S switches, wherein a
8 Kth one of said S switches in said Logic 1 switch array couples an
9 output of said Logic 1 input detector to a second input of said Kth
10 accumulator;

11 wherein said control circuitry is capable of synchronously applying
12 the M bits in said Kth orthogonal modulation code in said storage
13 array as a switch control signal to said Kth switch in said Logic 1
14 switch array so that each Logic 1 binary data in said Kth
15 orthogonal modulation code closes said Kth switch in said Logic 1
16 switch array, thereby connecting the output signal of said Logic 1
17 input detector to said second input of said Kth accumulator.

12. The CDMA wireless network as set forth in Claim 11 wherein each Logic 1 binary data in said Kth orthogonal modulation code opens said Kth switch in said Logic 0 switch array, thereby disconnecting the output signal of said Logic 0 input detector from said first input of said Kth accumulator.

13. The CDMA wireless network as set forth in Claim 12 wherein each Logic 0 binary data in said Kth orthogonal modulation code opens said Kth switch in said Logic 1 switch array, thereby disconnecting the output signal of said Logic 1 input detector from said second input of said Kth accumulator.

14. The CDMA wireless network as set forth in Claim 11 further comprising a code selection circuit capable of reading a sum value from each said S accumulators and identifying an accumulator containing a maximum sum value.

15. The CDMA wireless network as set forth in Claim 14 wherein said code selection circuit outputs one of 2^N N-bit data symbols corresponding to said identified accumulator contain said maximum value.

1 16. The CDMA wireless network as set forth in Claim 15
2 wherein $N = 6$ and $M = 2^N = 64$.

1 17. The CDMA wireless network as set forth in Claim 16
2 wherein $S = 64$.

1 18. The CDMA wireless network as set forth in Claim 17
2 wherein said orthogonal modulation codes are Walsh codes.

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1 19. For use in a base station of a wireless network capable
2 of communicating with mobile stations located in a coverage area of
3 the wireless network, a method of demodulating a set of S possible
4 orthogonal modulation codes received serially as binary data,
5 wherein each of the orthogonal modulation codes comprises M binary
6 bits representing an N-bit data symbol and wherein $M = 2^N$, the
7 method comprising the steps of:

8 in a Logic 0 input detector, comparing each of the M
9 binary bits of the serially received orthogonal modulation codes to
10 a Logic 0 and outputting a +1 signal if a match occurs and
11 outputting a -1 signal if a match does not occur;

12 retrieving from a storage array the Kth one of S
13 orthogonal modulation codes stored therein;

14 synchronously applying the M bits of the Kth orthogonal
15 modulation code as a switch control signal to a Kth switch in a
16 Logic 0 switch array comprising S switches, wherein the Kth switch
17 in the Logic 0 switch array is capable of coupling an output of the
18 Logic 0 input detector to a first input of a Kth one of S
19 accumulators, and wherein each Logic 0 binary data in the Kth
20 orthogonal modulation code closes the Kth switch in the Logic 0
21 switch array, thereby connecting the output signal of the Logic 0
22 input detector to the first input of the Kth accumulator.

1 20. The method as set forth in Claim 19 further comprising
2 the steps of:

3 in a Logic 1 input detector, comparing each of the M
4 binary bits of the serially received orthogonal modulation codes to
5 a Logic 1 and outputting a +1 signal if a match occurs and
6 outputting a -1 signal if a match does not occur;

7 synchronously applying the M bits of the Kth orthogonal
8 modulation code as a switch control signal to a Kth switch in a
9 Logic 1 switch array comprising S switches, wherein the Kth switch
10 in the Logic 1 switch array is capable of coupling an output of the
11 Logic 1 input detector to a second input of the Kth accumulator,
12 and wherein each Logic 1 binary data in the Kth orthogonal
13 modulation code closes the Kth switch in the Logic 1 switch array,
14 thereby connecting the output signal of the Logic 1 input detector
15 to the second input of the Kth accumulator.